Remarks:

Reconsideration of the application, as amended, is respectfully requested.

Claims 1 - 76 are presently pending in the application. Claims 1 - 38 are subject to examination and claims 39 - 76 have been withdrawn from examination. Claims 1 and 20 have been amended. Claims 77 - 78 were previously canceled. As it is believed that the claims were patentable over the cited art in their original form, the claims have not been amended to overcome the references.

In item 3 of the above-identified Office Action, claims 1 and 20 were rejected as allegedly being indefinite under 35 U.S.C. § 112, second paragraph, for using the phrase "configured in the **same ways** that". Applicants' claims 1 and 20 have been amended to address the concerns raised in item 3 of the Office Action.

The amendments to claims 1 and 20 are supported by the specification of the instant application, for example, on page 25 of the instant application, line 4 - page 26, line 2, which state:

> **The configuration of the configurable elements of the SLE layer,** i.e. the configuration of the multiplexers, the configurable connections within the structurable logic arrangements and the registers **can essentially be**

> **effected like the configuration of the known field-programmable logic arrangements (PLAs, GALs, PLDs, FPGAs etc.).**
>
> **A first possibility in this respect consists in the (irreversible) production or erasure of connections using so-called fuses or antifuses.**
>
> **Another possibility consists in carrying out reversible configuration based on data representing the desired configuration, the data being stored in EPROMS, EEPROMS** or the like provided inside or outside the program-controlled unit. As a result, the configuration of the program-controlled unit can be changed a limited number of times.
>
> **A further possibility consists in carrying out reversible configuration based on data representing the desired configuration, but where the data are stored in a RAM or the like.** As a result, the configuration of the program-controlled unit can be changed an unlimited number of times and very rapidly. [emphasis added by Applicant]

It is accordingly believed that the claims meet the requirements of 35 U.S.C. § 112, second paragraph.

In item 5 of the Office Action, claims 1 - 7, 10 - 11, 13 - 26, 29 - 30 and 32 - 38, were rejected under 35 U.S.C. § 103(a) as allegedly being obvious over U. S. Patent No. 6,598,148 to Moore et al ("**MOORE**") in view of U. S. Patent No. 6,279,045 to Muthujumaraswathy et al ("**MUTHUJUMARASWATHY**"). In item 22 of the Office Action, claims 8, 9, 12, 27, 28 and 31, were rejected under 35 U.S.C. § 103(a) as allegedly being obvious over **MOORE** in view of **MUTHUJUMARASWATHY**, and further in view of United States Patent No. 5,825,878 to Takahashi et al ("**TAKAHASHI**").

Applicant respectfully traverses the above rejections.

More particularly, claim 1 recites, among other limitations:

> an application-specifically **configurable intelligent interface** for respectively connecting said intelligent core and said plurality of units, . . . ;
>
> **said application-specifically configurable intelligent interface including a structurable hardware unit** including at least one of structurable data paths and structurable logic elements; and
>
> **said structurable hardware unit being configured using at least one of fuses, anti-fuses and data representing a desired reversible configuration being stored in a memory device**, to evaluate and process data and/or signals received. [emphasis added by Applicant]

Applicant's independent claim 20 recites similar limitations, among others.

As such, Applicant's particularly claimed **configurable intelligent interface** of claims 1 and 20 includes a **structurable hardware unit that can be configured using at least one of fuses, anti-fuses and data representing a desired reversible configuration being stored in a memory device**. However, none of the cited references teach or suggest, among other limitations, a **configurable intelligent interface**, as particularly claimed by Applicant.

More particularly, the **MOORE** reference fails to teach or suggest, among other limitations of Applicant's claims, **an application specifically configurable intelligent interface connecting the intelligent core to the plurality of units**, as particularly required by Applicant's claims 1 and 20.

Rather, pages 4 and 11 of the Office Action point to an "interface port, 423, fig 17" of **MOORE** as allegedly disclosing Applicant's claimed "application specifically **configurable intelligent interface**". Applicant respectfully disagrees.

Applicant notes that Fig. 17 of **MOORE** does not show an "interface port" "423". However, Applicant believes that the Office Action meant to refer to the "I/O Interface 432" of Fig. 17 of **MOORE**, and absent further clarification, reference to that "I/O Interface 432" will be made herein.

Applicant's independent claims 1 and 20 are patentable over the **MOORE** reference, alone or in combination with the other cited references, because, among other reasons, the "I/O Interface 432" of Fig. 17 of **MOORE** is not **configurable**, as required by Applicant's independent claims 1 and 20. This can be seen from Col. 14 of **MOORE**, line 62 - col. 15, line 20, which states:

ASYNCHRONOUS/SYNCHRONOUS CPU

Most microprocessors derive all system timing from a single clock. The disadvantage is that different parts of the system can slow all operations. **The microprocessor 50 provides a dual-clock scheme as shown in FIG. 17, with the CPU 70 operating asynchronously to I/O interface 432 forming part of memory controller 118 (FIG. 2) and the I/O interface 432 operating synchronously with the external world of memory and I/O devices.** The CPU 70 executes at the fastest speed possible using the adaptive ring counter clock 430. Speed may vary by a factor of four depending upon temperature, voltage, and process. The external world must be synchronized to the microprocessor 50 for operations such as video display updating and disc drive reading and writing. This synchronization is performed by the I/O interface 432, speed of which is controlled by a conventional crystal clock 434. **The interface 432 processes requests for memory accesses from the microprocessor 50 and acknowledges the presence of I/O data.** The microprocessor 50 fetches up to four instructions in a single memory cycle and can perform much useful work before requiring another memory access. **By decoupling the variable speed of the CPU 70 from the fixed speed of the I/O interface** 432, optimum performance can be achieved by each. **Recoupling between the CPU 70 and the interface 432 is accomplished with handshake signals** on lines 436, with data/addresses passing on bus 90, 136.

The above-cited portion of **MOORE**, describing the I/O interface 432 of Fig. 17 of **MOORE**, states that the I/O interface operates at a fixed speed, and that it can be coupled to and decoupled from the CPU 70. However, that it can be decoupled from and recoupled to the CPU does not make the **interface, itself, configurable**, as required by Applicant's claims 1 and 20. Further, the interface 432 of **MOORE** is not **an application specifically configurable intelligent interface connecting the intelligent core to the plurality of units**, as particularly required by Applicant's claims 1 and 20. The decoupling and

recoupling of the CPU from the fixed speed of the I/O interface 432 of **MOORE** neither teaches, nor suggests, among other limitations of Applicant's claims, an **application-specifically configurable intelligent interface connecting the intelligent core to the plurality of units and including a structurable hardware unit including at least one of structurable data paths and structurable logic elements**, as presently required by Applicant's claims 1 and 20.

First, the decoupling/recoupling of the clock speed of the CPU to the Interface 432, disclosed in **MOORE**, fails to teach or suggest, among other limitations of Applicant's claims 1 and 20, that the **interface is either merely configurable** or even **application specifically configurable**. Further, the decoupling/recoupling disclosed in **MOORE** fails to teach or suggest, among other limitations of Applicant's claims 1 and 20, that the **interface** is **configurable because it includes a structurable hardware unit including at least one of structurable data paths and structurable logic elements**, as currently recited in Applicant's amended claims 1 and 20.

Further still, as acknowledged on page 4 of the Office Action, **MOORE** fails to teach or suggest, among other limitations of Applicant's claims 1 and 20, that the hardware unit is configured "**said structurable hardware unit being configured**

using at least one of fuses, anti-fuses and data representing a desired reversible configuration being stored in a memory device". This failure of **MOORE** is acknowledged on page 4 of the Office Action. Rather, page 5 of the Office Action points to **MUTHUJUMARASWATHY**, in combination with **MOORE**, as allegedly disclosing a configurable interface including a structurable hardware unit that is configured in the same ways as field-programmable logic arrangements. Applicant respectfully disagrees.

Like **MOORE**, **MUTHUJUMARASWATHY** fails to teach or suggest, among other limitations of Applicant's claims, **an application-specifically configurable intelligent interface connecting the intelligent core to the plurality of units and including a structurable hardware unit**, as required by Applicant's independent claims 1 and 20. As such, the **MUTHUJUMARASWATHY** reference cannot cure this deficiency in the teachings of **MOORE**. Additionally, since **MUTHUJUMARASWATHY** does not teach or suggest a **configurable intelligent interface, as claimed by Applicant's claims 1 and 20, MUTHUJUMARASWATHY** also **cannot** be said to teach or suggest, among other limitations of Applicant's claims, a **configurable intelligent interface including at least one of structurable data paths and structurable logic elements, configured using at least one of**

fuses, anti-fuses and data representing a desired reversible configuration being stored in a memory device.

Further, like **MOORE**, **MUTHUJUMARASWATHY** also fails to teach or suggest, among other limitations of Applicant's claims, an **application-specifically configurable** intelligent **interface** connecting an intelligent core to a plurality of units. Further, **MUTHUJUMARASWATHY** fails to teach or suggest, among other limitations of Applicant's claims **an interface that includes at least one of structurable data paths and structurable logic elements, configured using at least one of fuses, anti-fuses and data representing a desired reversible configuration being stored in a memory device**

Instead, **MUTHUJUMARASWATHY** discloses a multimedia interface having a multimedia processor and a field programmable gate array (FPGA). Although **MUTHUJUMARASWATHY** discloses that the invention, in its entirety, is directed towards a multimedia interface, it does **not** teach or suggest, that the interface is application specifically configurable to connect an intelligent core to a plurality of units. Rather, in **MUTHUJUMARASWATHY**, the "interface" disclosed in the title and abstract is **the core, FPGA and the units**, and **not** an interface connected **between** a core and a plurality of units, as required by Applicant's claims 1 and 20. Further, the FPGA in

MUTHUJUMARASWATHY is **not** an **interface** between an intelligent core and a plurality of units, as claimed by Applicant's claims 1 and 20.

In view of the foregoing, it can be seen that the **MOORE** and **MUTHUJUMARASWATHY** references, taken alone or in combination, fail to teach or suggest all limitations of Applicant's claims 1 and 20. For example, the combination of **MOORE** and **MUTHUJUMARASWATHY** still fails to teach or suggest, among other limitations of Applicant's claims, the **particularly** claimed application specifically **configurable** intelligent **interface** (i.e., including a **structurable** hardware unit), of Applicant's amended claims 1 and 20. Thus, Applicant's claims 1 and 20 are believed to be patentable over the **MOORE** and **MUTHUJUMARASWATHY** references.

The **TAKAHASHI** reference, cited in the Office Action in combination with **MOORE** and **MUTHUJUMARASWATHY** against certain of Applicant's dependent claims, does not cure the above-discussed deficiencies in the **MOORE** and **MUTHUJUMARASWATHY** references.

It is accordingly believed that none of the references, whether taken alone or in any combination, teach or suggest the features of claims 1 and 20. Claims 1 and 20 are,

therefore, believed to be patentable over the art. The dependent claims currently being examined are believed to be patentable as well because they all are ultimately dependent on claims 1 or 20.

In view of the foregoing, reconsideration and allowance of claims 1 - 76 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

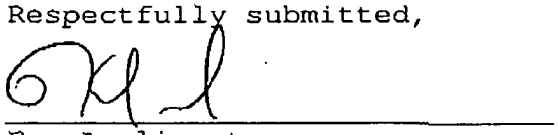
Additionally, please consider the present as a petition for a one (1) month extension of time, and please provide a one (1) month extension of time, to and including, January 22, 2008 to respond to the present Office Action.

The extension fee for response within a period of one (1) month pursuant to Section 1.136(a) in the amount of $120.00 in accordance with Section 1.17 is enclosed herewith.

Please provide any additional extensions of time that may be necessary and charge any other fees that might be due with

respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemer LLP, No. 12-1099.

Respectfully submitted,



For Applicant

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January 22, 2008

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